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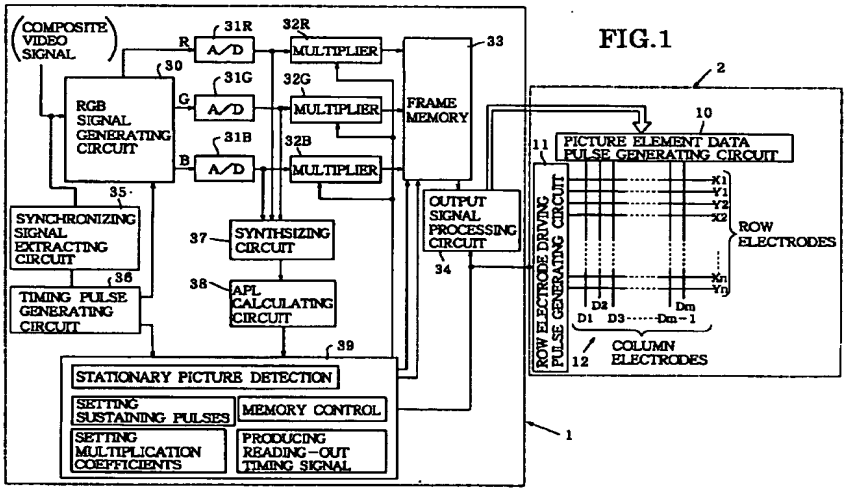
(54) Method of and system for controlling brightness of plasma display panel

(57) A method of and a system for controlling a brightness of a picture displayed on a plasma display panel are provided which are capable of determining whether a video signal to be fed to the plasma display panel is a signal indicating a stationary picture, reducing the brightness of a picture displayed on the plasma display panel if it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture.

FIG.1



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a method of and a system for controlling the brightness of a plasma display panel (hereinafter referred to as PDP), particularly for controlling the brightness of a picture reproduced from video signals and displayed on the PDP.

[0002] Fig. 10 is an explanatory view indicating a conventional driving system for driving an AC discharge type PDP whose luminescent units are arranged in a matrix manner.

[0003] As shown in Fig. 10, the conventional driving system has a signal processing section 1 for processing inputted composite video signals and for producing DVD driving signals, a display section 2 for receiving the DVD driving signals fed from the signal processing section 1 and for displaying reproduced picture on the PDP.

[0004] In the signal processing section 1, composite video signals inputted from the outside are processed in an A/D converter 3, so that said video signals will become in synchronism with a timing pulse produced from a timing pulse generating circuit 7, and are converted into 8-bit digital picture element data signals which are then fed to a frame memory 4.

[0005] The frame memory 4, in accordance with a taking-in signal and a reading-out signal both of which are all fed from a memory control circuit 8, is adapted to successively take-in picture element data from the digital picture element data signal fed from the A/D converter 3, and to read-out the taken-in picture element data which is then fed to an output signal processing circuit 5.

[0006] The output signal processing circuit 5 is provided to process the digital picture element data signal so as to produce for each field a picture element data signal having a mode (8 bit) corresponding to a brightness gradation of the filed. Then, the picture element data signal is synchronized with a timing signal fed from a timing signal generating circuit 9 and is further fed to a picture element data pulse generating circuit 10.

[0007] In the signal processing section 1, composite video signals inputted from the outside are also fed to a synchronizing signal separation circuit 6 which is provided to extract a horizontal synchronizing signal and a vertical synchronizing signal from the composite video signals. The extracted horizontal synchronizing signal and vertical synchronizing signal are then supplied to a timing pulse generating circuit 7.

[0008] The timing pulse generating circuit 7 is provided to produce various timing pulses in accordance with the above horizontal and vertical synchronizing signals. The various timing pulses are fed to the A/D converter 3, a memory control circuit 8 and a reading-out timing signal generating circuit 9.

[0009] Here, the A/D converter 3 is provided to, in synchronism with the timing pulse fed from the timing pulse generating circuit 7, perform analog/digital conversion for the composite video signals fed from the outside to the signal processing section 1.

[0010] The memory control circuit 8 is provided to produce a taking-in signal (in synchronism with a timing pulse fed from the timing pulse generating circuit 7) and a reading-out signal (in synchronism with a reading-out timing signal fed from the reading-out timing signal generating circuit 9) to the frame memory 4. Accordingly, the frame memory 4 can take-in picture element data from digital picture element data signal fed from the A/D converter 3, and can read-out the taken-in picture element data.

[0011] The reading-out timing signal generating circuit 9 receives a timing pulse fed from the timing pulse generating circuit 7, and produces a reading-out timing signal in accordance with said timing pulse. The reading-out timing signal is fed to the memory control circuit 8, the output signal processing circuit 5, further to a row electrode driving pulse generating circuit 11 of the display section 2.

[0012] In this way, the memory control circuit 8 can produce a reading-out signal to the frame memory 4, and the output signal processing circuit 5 can produce picture element data to a picture element data pulse generating circuit 10 of the display section 2.

[0013] Referring to Fig. 11, the display section 2 comprises a PDP 12 which includes a plurality of row electrodes Xi, Yi (i=1, 2. . . n) arranged in parallel with one another on an inner surface of a front glass substrate 12A serving as a picture display panel.

[0014] Further, a dielectric layer 12B is provided to cover the row electrodes Xi, Yi (i=1, 2. . . n). A magnesium oxide (MgO) layer 12C is formed on the dielectric layer 12B, an electric discharge space 12E is formed between the magnesium oxide layer 12C and a rear glass substrate 12D.

[0015] A plurality of column electrodes Dj (j=1, 2. . . m) are arranged in parallel with one another on an inner surface of the rear glass substrate 12D, in a manner such that the column electrodes Dj (j=1, 2. . . m) are perpendicular to the row electrodes Xi, Yi (i=1, 2. . . n).

[0016] In practice, each pair of row electrodes Xi, Yi are used to form one displaying line within the PDP, each intersection formed by one pair of row electrodes Xi, Yi with one column electrode Dj forms a picture element cell.

[0017] The picture element data pulse generating circuit 11 of the display section 2 is connected with the plurality of column electrodes Dj (j=1, 2. . . m) for producing picture element data pulses DPj (j=1, 2. . . m) corresponding to the picture element data fed from the output signal processing circuit 5 of the signal processing section 1, said picture element data pulses DPj (j=1, 2. . . m) being applied to the column electrodes Dj (j=1, 2. . . m).

[0018] The row electrode driving pulse generating circuit 11 is connected with the plurality of row electrodes

Xi, Yi (i=1, 2. . . n), so as to produce the following pulses to these row electrodes Xi, Yi (i=1, 2. . . n) in accordance with the reading-out timing signals fed from the reading-out timing signal generating circuit 9 of the signal processing section 1. In fact, the pulses produced by the row electrode driving pulse generating circuit 11 and fed to the plurality of row electrodes Xi, Yi (i=1, 2. . . n), are reset pulses RPx, RPy for effecting an electric discharge between each pair of row electrodes Xi, Yi (i=1, 2. . . n) to generate charged particles in the discharge space 12E, priming pulses PP for reforming the charged particles, scanning pulses SP for writing-in picture element data, sustaining pulses LPx, LPy for maintaining discharge luminescence, erasing pulses EP for erasing wall electric charges.

[0019] Fig. 12 is a timing chart indicating various timings of the above pulses to be applied to the row electrodes Xi, Yi (i=1, 2. . . n).

[0020] As shown in Fig. 12, a reset pulse RPx of a positive voltage is applied to each of the row electrodes Xi (i=1, 2. . . n), while another reset pulse RPy of a negative voltage is applied to each of the row electrodes Yi (i=1, 2. . . n). With the application of the reset pulses RPx and RPy, an electric discharge is induced in a space between each pair of row electrodes Xi, Yi (i=1, 2. . . n), whereby generating charged particles within the electric discharge space 12E corresponding to all the picture element cells.

[0021] By virtue of the charged particles, upon completion of the electric discharge, a predetermined amount of wall charges will form in the same manner in all the picture element cells within the dielectric layer 12B.

[0022] Here, a time period until the formation of the wall charges is called an all-at-once reset period.

[0023] On the other hand, the picture element data pulse generating circuit 10 operates to successively apply picture element data pulses DPj (j=1, 2. . . m) (each having a voltage corresponding to picture element data) to the column electrodes Dj (j=1, 2. . . m).

[0024] As shown in Fig. 12, just before the picture element data pulse generating circuit 10 applies picture element data pulse DPj (j=1, 2. . . m) to the column electrodes Dj (j=1, 2. . . m), the row electrode driving pulse generating circuit 11 applies a priming pulse PP of a positive polarity to each of the row electrodes Yi (i=1, 2. . . n). Then, a scanning pulse SP having a predetermined small pulse period and a negative polarity is successively applied to each of the row electrodes Yi (i=1, 2. . . n), in synchronism with a timing of the picture element data pulse DPj (j=1, 2. . . m).

[0025] With the application of the priming pulse PP, the charged particles formed in the all-at-once reset period but have decreased with the passing of time, can be increased again. Further, when the scanning pulses SP are applied during a period the charged particles are still existing, an electric potential difference between a scanning pulse SP and a picture element data pulse DPj will occur, causing a selected discharge therebetween, thereby effecting a predetermined writing-in of the picture element data.

[0026] Namely, a scanning pulse SP can serve as a trigger for selectively erasing (corresponding to picture element data) wall charges formed due to charged particles in each picture element cell within the dielectric layer 12B, thereby effecting a predetermined writing-in of the picture element data, depending upon whether or not electric discharges are caused between the row electrodes Yi (i=1, 2. . . n) and the column electrodes Dj (j=1, 2. . .m) and wall electrodes are thus erased.

[0027] For example, the voltage of each of the picture element data pulses DPj (j=1, 2. . .m) applied to a picture element cells will be V (having a positive polarity) if a picture element data indicates a logic "1", but will be 0 if a picture element data shows a logic "0". On a line within the PDP 12 to which a scanning pulse SP is applied, when a picture element data indicates a logic "1", an electric potential difference between a scanning pulse SP and a picture element data pulse DPj (j=1, 2. . . m) becomes large, thus there will be a minor electric discharge (corresponding to the period of a scanning pulse SP) between a row electrode Yi and a column electrode Dj, thereby erasing wall charges in the dielectric layer 12B corresponding to picture element cells. At this moment, since a time for the electric discharge is short, there would be no wall charges newly formed in the dielectric layer 12B.

[0028] On the other hand, when the picture element data (corresponding to picture element cell) indicates a logic "0", an electric potential difference between a scanning pulse SP and a picture element data pulse DPj (j=1, 2. . . m) is small. As a result, there will not be any electric discharge between a row electrode Yi and a column electrode Dj, rendering wall charges to remain within the dielectric layer 12B corresponding to picture element cells.

[0029] Here, a period necessary for writing-in the picture element data by virtue of the erasing of the wall charges is called an address period.

[0030] Next, the row electrode driving pulse generating circuit 11 operates to continuously apply a sustaining pulse LPx of positive polarity to each row electrode Xi, and continuously apply a sustaining pulse LPy of positive polarity to each row electrode Yi in a timing slightly later than a timing for applying the pulse LPx.

[0031] With the application of the sustaining pulses LPx and LPy, discharge luminescence occurs only in picture element cells where wall charges are remaining within the dielectric layer 12B. Such discharge luminescence may be maintained during a period when the sustaining pulses LPx and LPy are being applied continuously.

[0032] By virtue of such discharge luminescence, a picture will then be displayed on the PDP 12.

[0033] Here, a period during which the discharge luminescence is maintained by continuously applying sus-

taining pulses LPx and LPy is called a discharge maintaining period.

[0034] After the discharge luminescence has been maintained for a predetermined period, the row electrode driving pulse generating circuit 11 operates to apply an erasing pulse EP having a negative polarity to each row electrode Yi, so as to erase the wall charges remaining in the dielectric layer 12B, thereby finishing the display of one field of picture.

[0035] However, with an AC discharge type matrix display PDP, since there is a significant temperature difference between portions of discharge luminescence and the portions of non-discharge luminescence, a problem such as cracking might occur on the PDP.

[0036] In order to prevent a possible cracking on a PDP, there has been suggested an Automatic Brightness/Beam Limiter for limiting a picture brightness when displaying a stationary picture on a display panel, as disclosed in the applicant's earlier application (Japanese Patent Application No. 9-187827).

[0037] Fig. 13 is a block diagram indicating a brightness limiting system disclosed by the applicant in the above-mentioned earlier application. With such a brightness limiting system, a composite video signal is decomposed into various analogue color signals R, G, B (Red, Green, Blue) by virtue of a color signal generating circuit (not shown).

[0038] As shown in Fig. 13, the color signals R, G, B are applied to A/D converters 20R, 20G, 20B to be converted into digital signals which are further fed to multipliers 21R, 21G, 21B in which each digital signal is multiplied by a multiplication coefficient, thereby setting brightness levels of various color signals R, G, B.

[0039] The various color signals R, G, B, whose brightness levels have been set, are fed to a frame memory (not shown) and further to an output signal processing circuit (not shown) so as to be applied to a display section (not shown), in the same manner as shown in Fig. 10.

[0040] However, the multiplication coefficients for use in setting the brightness levels of various color signals R, G, B may be determined in the following way.

[0041] Namely, color signals R, G, B, which have been converted into digital signals in A/D converters 20R, 20G and 20B, are fed to a synthesizing circuit 22 so as to be synthesized with a brightness signal. The systhesized signal is then fed to an APL (Average Picture Level) calculating circuit 23.

[0042] The APL calculating circuit 23 is provided to divide video signal of one field picture into eight blocks in vertical direction (see Fig. 14) and to calculate an APL value for each block. The APL values are then fed to an APL adder circuit 24.

[0043] The APL adder circuit 24 is provided to adder together the APL values of two adjacent blocks to obtain an added APL value to be fed to a comparator circuit 25.

[0044] The comparator circuit 25 is provided to compare an added APL value with a reference value set in advance in a reference value generating circuit 26, with a comparing result fed to a multiplication coefficient setting circuit 27.

[0045] The multiplication coefficient setting circuit 27 operates to set multiplication coefficients for multipliers 21R, 21G, 21B, in accordance with comparison results fed from the comparator circuit 25. Namely, if an added APL value is larger than a reference value, a multiplication coefficient (preset in the circuit 27 and smaller than 1), will be fed to each of the multipliers 21R, 21G, 21B. The multipliers 21R, 21G, 21B will thus operate to multiply the color signals R, B, G with the multiplication coefficient, so as to reduce the brightness level of color signals R, B, G.

[0046] On the other hand, if each of added APL values is smaller than a reference value, a multiplication coefficient (preset in the circuit 27 and equal to 1), will be fed to each of the multipliers 21R, 21G, 21B, so as not to reduce the brightness level of color signals R, B, G.

[0047] For instance, if a reference value preset in the circuit 26 is 400, in a pattern of Fig. 14A (in which numerical numbers are used to represent APL values of the blocks), since each of added APL values of two adjacent blocks is smaller than 400, only a multiplication coefficient equal to 1 is outputted from the multiplication coefficient generating circuit 27, so as not to reduce the brightness level of color signals R, B, G.

[0048] On the other hand, as shown in a pattern of Fig. 14B, if an added APL value of two adjacent blocks (block 4 and block 5) is larger than the preset reference value 400, multiplication coefficient preset in the circuit 27 and smaller than 1 (for example 0.5), will be fed to the multipliers 21R, 21G, 21B. The multipliers 21R, 21G, 21B will operate to multiply the color signals R, B, G with the multiplication coefficient (0. 5), so as to reduce the brightness level of various color signals, as shown in Fig. 14C (APL value of each block has been reduced to 1/2 of its original value).

[0049] With the use of the above brightness control system, it is possible to reduce the picture brightness on some areas of a PDP where bright picture portions are collected, thereby preventing occurence of cracking on the PDP.

[0050] However, it has been proved that the above conventional brightness control system (Automatic Brightness/Beam Limiter) is effective only in a case where a bright portion α of a stationary picture is collecte in a leteral direction (see Fig. 15), but is not effective in a case where a bright portion α of a stationary picture is collected in a vertical direction (see Fig. 16). The reason responsible for the case of Fig. 16 is that APL values of all the blocks are low, an added APL value of every two adjacent blocks is lower than a predetermined reference value, hence disabling the brightness control system (Automatic Brightness/Beam Limiter), and making it impossible to prevent a cracking in a PDP.

SUMMARY OF THE INVENTION

[0051] It is an object of the present invention to provide an improved method of controlling the brightness of a PDP (plasma display panel), capable of preventing a cracking on the PDP, regardless of what pattern of a stationary picture is displayed on the PDP, thereby solving the above-mentioned problems peculiar to the above-discussed prior arts.

[0052] According to the present invention, there is provided a method of controlling a brightness of a picture displayed on a plasma display panel by increasing or decreasing said brightness, said method comprising: determining whether a video signal to be fed to the plasma display panel is a signal indicating a stationary picture; reducing the brightness of a picture displayed on the plasma display panel if it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture.

[0053] In one aspect of the present invention, one average brightness level of a video signal to be fed to the plasma display panel is detected during a predetermined period, said one average brightness level is then compared with a former average brightness level detected immediately before the detection of said one average brightness level, so as to obtain a difference between said one average brightness level and said former average brightness level.

[0054] In another aspect of the present invention, when the difference between said one average brightness level and said former average brightness level is smaller than a predetermined value and such condition has continued for a predetermined time, it is determined that said video signal is a signal indicating a stationary picture.

[0055] In a further aspect of the present invention, when it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture, the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel is reduced.

[0056] In a still further aspect of the present invention, the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel is reduced gradually step by step.

[0057] In one more aspect of the present invention, when it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture, multiplication coefficients are made smaller which will be multiplied with video signals to be fed to the plasma display panel to adjust the brightness of the stationary picture displayed on the plasma display panel.

[0058] Further, according to the present invention, there is provided a system for controlling a brightness of a picture displayed on a plasma display panel by increasing or decreasing said brightness, said system comprising: determining means for determining whether a video signal to be fed to the plasma display panel is a signal indicating a stationary picture; brightness reducing means for reducing the brightness of a picture displayed on the plasma display panel if it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture.

[0059] In one more aspect of the present invention, the above determining means comprises: average brightness level detecting means for detecting during a predetermined period one average brightness level of a video signal to be fed to the plasma display panel; calculating means for comparing said one average brightness level with a former average brightness level detected immediately before the detection of said one average brightness level and for obtaining a difference between said one average brightness level and said former average brightness level; monitor means for monitorring whether the difference obtained by the calculating means has continuously been smaller than a predetermined value for a predetermined time. In particular, when the monitor means determines that the difference obtained by the calculating means has continuously been smaller than a predetermined value for a predetermined time, it is determined that said video signal is a signal indicating a stationary picture.

[0060] In still one more aspect of the present invention, the brightness reducing means is means capable of reducing the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel.

[0061] In still one more aspect of the present invention, the brightness reducing means is capable of reducing the number of the sustaining pulses gradually step by step.

[0062] In still one more aspect of the present invention, the brightness reducing means is means capable of reducing multiplication coefficients to be multiplied by video signals to be fed to the plasma display panel so as to adjust the brightness level of the video signals.

[0063] The above objects and features of the present invention will become better understood from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0064]

Fig. 1 is a block diagram indicating a system of the present invention for controlling the brightness of a plasma display panel.

Fig. 2 is a flowchart indicating a procedure for determining whether a picture displayed on a display is a stationary picture.

Fig. 3 is a flowchart indicating a procedure for reducing the brightness of the plasma display panel.

Fig. 4 is a flowchart indicating another procedure

for reducing the brightness of the plasma display panel.

Fig. 5 is a flowchart indicating a procedure for increasing the brightness of the plasma display panel.

Fig. 6 is a flowchart indicating another procedure for increasing the brightness of the plasma display panel.

Fig. 7 is a graph indicating a condition where the number of sustaining pulses is reduced by using a procedure shown in Fig. 3.

Fig. 8 is an explanatory view indicating one frame picture on gradation display.

Fig. 9 is a graph indicating performance of stationary picture and performance of ABL when multiplication coefficients are reduced by using a procedure shown in Fig. 4.

Fig. 10 is a block diagram indicating a system of a prior art for controlling the brightness of a plasma display panel.

Fig. 11 is a perspective view indicating the structure of a plasma display panel to be driven by using a method and a system according to a prior art.

Fig. 12 is a timing chart indicating a timing for applying various pulses to the plasma display panel, using a method according to a prior art.

Fig. 13 is a block diagram indicating a system for driving a plasma display panel, according to a prior art.

Fig. 14 is used to indicate how to reduce the brightness of a plasma display panel using a method and a system according to a prior art.

Fig. 15 is an explanatory view indicating one example of a picture pattern of a stationary picture.

Fig. 16 is an explanatory view indicating another example of a picture pattern of a stationary picture.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0065] Referring to Fig. 1, a PDP driving system in which the present invention has been applied, includes a signal processing section land a display section 2.

[0066] The signal processing section 1 comprises an RGB (Red, Green, Black) color signal generating circuit 30 capable of separating a composite video signal (fed from the outside) into various analogue color signals (Red, Green, Black), A/D converters 31R, 31G, 31B for converting various analogue color signals of PGB into digital signals, multipliers 32R, 32G, 32B for multiplying the digital color signals R, G, B with required multiplication coefficient, a frame memory 33 capable of taking-in picture element data from the digital color signals (multiplied with the multiplication coefficient) and capable of reading-out the picture element data, an output data processing circuit 34 capable of converting digital signal of picture element data read from the frame memory 33 into picture element data signal of a mode (8 bit) corresponding to a brightness gradation in each field and capable of feeding such picture element data signal into the display section 2, a synchronizing signal extracting circuit 35 capable of extracting a horizontal synchronizing signal and a vertical synchronizing signal from the composite video signal, a timing pulse generating circuit 36 for generating a timing pulse in accordance with the extracted horizontal synchronizing signal and a vertical synchronizing signal, a synthesizing circuit 37 for synthesizing the digital color signals R, G, B to produce a brightness signal, an APL (Average Picture Level) calculating circuit 38 for calculating an APL (for every vertical scanning period) in accordance with the brightness signal, and a controller 39 capable of determining whether a picture displayed on the PDP is a stationary picture so as to set a multiplication coefficient in accordance with the calculated APL, and capable of controlling an operation timing of the frame memory 33, the output signal processing circuit 34 and the display section 2.

[0067] The display section 2 is just the same as that discussed in prior art shown in Fig. 10, including a picture element data pulse generating circuit 10, a row electrode driving pulse generating circuit 11, and a PDP 12.

[0068] Here, the synchronizing signal extracting circuit 35 can extract a horizontal synchronizing signal and a vertical synchronizing signal from the composite video signal and apply these synchronizing signals to the timing pulse generating circuit 36. The timing pulse generating circuit 36 then generates the timing pulse in accordance with the horizontal synchronizing signal and the vertical synchronizing signal and applies the timing pulse to the RGB generating circuit 30 and controller 39.

[0069] The RGB generating circuit 30 is provided to separate the composite video signal into RGB analogue signals in synchronism with the timing pulse fed from the timing pulse generating circuit 36.

[0070] Then, the color signals R, G, B are applied to A/D converters 31R, 31G, 31B to be converted into digital signals which are further fed to multipliers 32R, 32G, 32B in which each digital signal is multiplied with a multiplication coefficient, thereby setting brightness levels of various color signals R, G, B.

[0071] The various digital color signals R, G, B, whose brightness levels have been set, are fed to the frame memory 33, and their picture element data are successively fed to the frame memory 33 in synchronism with taking-in signal supplied from the controller 39.

[0072] The picture element data fed into the frame memory 33 are then read out therefrom in synchronism with reading-out signal fed from the controller 39, and fed to the output data processing circuit 34 in which the picture element data are converted into picture element data signal of a mode (8 bits) corresponding to brightness gradation in each field. The picture element data signal are fed to the picture element data pulse generating circuit 10 of the display section 2, in synchronism with reading-out timing signal fed from the controller 39.

[0073] The controller 39 is capable of determining whether a picture displayed on the PDP of the display section 2 is a stationary picture or not, and thus controlling the brightness of the PDP 12 in accordance with the result of said determination.

[0074] Namely, the digital color signals R, G, B supplied from the A/D converters 31R, 31G, 31B are fed into the synthesizing circuit 37 in which these digital color signals are combined with brightness signal, and the combined signal is supplied to the APL calculating circuit 38.

[0075] The APL calculating circuit 38 can calculate an APL in every vertical scanning period for displaying a picture on the PDP, while a signal indicating the calculated APL value is fed to the controller 39.

[0076] Referring to Fig. 1, the controller 39 is fabricated so that it is capable of determining whether a picture displayed on the PDP is a stationary picture, with the determination being conducted in accordance with the calculated APL; setting the number of sustaining pulse to be fed from the row electrode driving pulse generating circuit 11, in accordance with the result of said determination; setting multiplication coefficient to be multiplied by the digital color signals R, G, B in the multipliers 32R, 32G, 32B, also in accordance with the result of the above determination.

[0077] Further, the controller 39 has a memory control function and a reading-out timing signal generating function. The memory control function is capable of controlling a timing for the frame memory 33 to take-in picture element data from the digital colour signals R, G, B and controlling a timing for reading-out the picture element data. The reading-out timing signal generating function is capable of producing a reading-out timing signal to be fed to the output signal processing circuit 34 and the row electrode driving pulse generating circuit 11 of the display section 2, corresponding to the number of timing pulses fed from the timing pulse generating circuit 36 or the number of sustaining pulses which have been set in advance.

[0078] A procedure for brightness control effectable by using the controller 39 may be described with reference to flowcharts shown in Figs. 2 - 6.

[0079] Referring to Fig. 2, the controller 39 operates to store an APL value (of every vertical scanning period) fed from the APL calculating circuit 38, and to calculate a difference ΔAPLn (APLt - APLt+1) between the APL value fed at this time and an APL value fed at the last time (step S1). Then, the difference ΔAPLn is compared with a reference value Vref set in advance so as to determine whether the difference ΔAPLn is larger or smaller than the reference value Vref (step S2).

[0080] If it is determined that the ΔAPLn is smaller than the reference value Vref, it is further determined whether said determination indicating the difference ΔAPLn is smaller than the reference value Vref has been repeated for n times (step S3).

[0081] If it is determined at step S3 that said determination indicating the difference ΔAPLn is smaller than the reference value Vref has not been repeated for n times, the program goes back to step s1 to repeat the process beginning with the step S1. On the other hand, if it is determined at step S3 that said determination indicating the difference ΔAPLn is smaller than the reference value Vref has been repeated for n times, it is allowed to determine that the picture displayed on the PDP 12 is a stationary picture, thereby executing a brightness reducing treatment (step S4) that will be described in detail later.

[0082] Afterwards, a counter is reset (step S5) for counting the number of times for the determination executed at step S3, while the program returns to step S1 so as to repeat the process beginning with the step S1.

[0083] On the other hand, if it is determined at step S2 that the ΔAPLn is larger than the reference value Vref, it is further determined whether said determination indicating the difference ΔAPLn is larger than the reference value Vref has been repeated with a predetermined frequency in a predetermined period. If it is determined that said determination indicating the difference ΔAPLn is larger than the reference value Vref has been repeated with a predetermined frequency in a predetermined period, it is allowed to determine that the picture displayed on the PDP 12 is a motion picture (step S6).

[0084] If it is determined at step S6 that said determination indicating the difference ΔAPLn is larger than the reference value Vref has not been repeated with a predetermined frequency in a predetermined period, the program goes back to step S1 to repeat the process beginning with the step S1.

[0085] If it is determined at step S6 that the picture displayed on the PDP 12 is a motion picture, it is further determined at a step S7 whether a brightness reducing treatment at step S4 is just in a process of being executed.

[0086] If it is determined at the step S7 that a brightness reducing treatment at step S4 is not in a process of being executed, the program goes back to step S1 to repeat the process beginning with the step S1. On the other hand, if it is determined that a brightness reducing treatment at step S4 is just in a process of being executed, said brightness reducing treatment is stopped and a brightness increasing treatment is executed at step S8.

[0087] Then, a counter is reset (step S9) for counting the frequency of determination executed at step S6, while the program returns to step S1 so as to repeat the process beginning with the step S1.

[0088] A procedure for brightness reducing treatment performed at step S4 may be described in the following.

[0089] In fact, there are two kinds of methods for performing the brightness reducing treatment, with one being shown in Fig. 3 and the other in Fig. 4. In detail, the two methods may be mutually changed-over automatically or manually.

[0090] In a method shown in Fig. 3, the number of sus-

taining pulses applied from the row electrode driving pulse generating circuit 11 to the row electrodes Xi, Yi (i=1, 2. . . n) of the PDP 12 is reduced so as to reduce the number of times for discharge luminescence, thereby reducing the brightness of a picture displayed on the PDP 12.

[0091] Namely, once the brightness reducing treatment at step S4 in Fig. 2 is decided to be executed, the number of sustaining pulses is set (step a1 in Fig. 3) at a brightness reducing value Nref which is lower than an initial value N1 for indicating a motion picture.

[0092] Then, it is determined at step a2 whether the number of the sustaining pulses applied from the row electrode driving pulse generating circuit 11 to the row electrodes Xi, Yi (i=1, 2 . . . n) of the PDP 12 has been set at the brightness reducing value Nref (step a2).

[0093] If it is determined at the step a2 that the number of the sustaining pulses has already been set at the brightness reducing value Nref, it is understood that the brightness reducing treatment is just in its process of being executed. On the other hand, if it is determined at step a2 that the number of the sustaining pulses has not been set at the brightness reducing value Nref, the row electrode driving pulse generating circuit 11 is controlled (at step a3) to reduce the number of sustaining pulses being applied to PDP 12 by a predetermined number, in accordance with a reading-out timing signal applied to the row electrode driving pulse generating circuit 11.

[0094] Then, it is determined at a step a4 whether a predetermined time for reducing the number of sustaining pulses has passed. If it is determined that said predetermined time has passed, the program returns to the step a2 so as to repeat the process beginning with step a2.

[0095] However, when the program is at the step a3, it is required that the number of sustaining pulses should not be reduced all at once. Further, a step (to determine whether a predetermined time for reducing the number of sustaining pulses has passed) performed at at step a4 is useful in obtaining an effect that the reduction of the number of the sustaining pulses will be gradual as shown in Fig. 7, thereby preventing a sudden darkening of a picture displayed on the PDP 12.

[0096] Subsequently, the steps a2 - a4 are repeated so that the number of sustaining pulses fed from the row electrode driving pulse generating circuit 11 is reduced gradually. At this moment, if it is determined at the step a2 that the number of the sustaining pulses has been reduced to the brightness reducing value Nref, the reducing process is stopped, so that the number of the sustaining pulses are maintained at the brightness reducing value Nref.

[0097] Here, if the PDP driving system employs a gradation displaying method involving the use of sub-fields, it is particularly important that the number of sustaining pulses be gradually reduced to a brightness reducing value set in advance.

[0098] For example, in a case of 256-step gradation display shown in Fig. 8, one frame has 8 sub-fileds SFr (r=1, 2. . . 8), including address periods Ar (r=1, 2. . . 8) and sustaining discharge period Sr (r=1, 2. . . 8). The number of sustaining discharges during the sustaining discharge periods Sr (r=1, 2. . .8) of 8 sub-fileds SFr (r=1, 2. . . 8), may be set to be in a ratio of 1 : 2 : 4 : 8 : 16 : 64 : 128.

[0099] The number of sustaining discharges during sustaining discharge periods Sr (r=1, 2. . . 8) are proportional to the brightness of PDP. Thus, by properly selecting sub-fields for sustaining discharge, it is allowed to obtain a desired brightness of 256 steps.

[0100] Therefore, in the PDP driving system employing a gradation displaying method, the number of sustaining discharge (the number of sustaining pulse) in each sub-field may be reduced to a brightness reducing value set in advance for each sub-field, it is sure to perform a desired brightness reducing treatment.

[0101] In a method shown in Fig. 4 which employs a forced operation of ABL (Automatic Brightness Limiter), the multiplication coefficients to be multiplied with digital color signals R, G, B are made small.

[0102] Namely, once the brightness reducing treatment at step S4 in Fig. 2 is decided to be executed, multiplication coefficients to be multiplied with the digital color signals R, G, B in the multipliers 32R, 32G, 32B are each set (step b1 in Fig. 4) at a brightness reducing multiplication coefficient Kref which is lower than an initial value K1 for indicating a motion picture.

[0103] Then, it is determined at a step b2 whether the multiplication coefficients set in the multipliers 32R, 32G, 32B are each equal to the brightness reducing muliplication coefficient Kref.

[0104] If it is determined at the step b2 that the multiplication coefficients set in the multipliers 32R, 32G, 32B are each equal to the brightness reducing multiplication coefficient Kref, it is understood that the brightness reducing treatment is just in its process of being executed. On the other hand, if it is determined at step b2 that the multiplication coefficients set in the multipliers 32R, 32G, 32B are not equal to the brightness reducing multiplication coefficient Kref, the multiplication coefficients to be multiplied with digital color signals R, G, B in the multipliers 32R, 32G, 32B are each reduced by a predetermined value (step b3).

[0105] Then, it is determined at a step b4 whether a predetermined time for reducing the multiplication coefficients has passed. If it is determined that said predetermined time has passed, the program returns to the step b2 so as to repeat the process beginning with step b2.

[0106] However, when the program is at the step b3, it is required that the multiplication coefficients to be multiplied with digital color signals R, G, B in the multipliers 32R, 32G, 32B should not be reduced to be equal to the brightness reducing multiplication coefficient Kref all at once. Further, an operation (to determine whether

a predetermined time for reducing the multiplication coefficients has passed) performed at the step b4 is useful in obtaining an effect of preventing a sudden darkening of a picture displayed on the PDP 12 by avoiding a sudden reduction in the brightness. Fig. 9 is a graph indicating a performance of a stationary picture and a performance of ABL at this moment.

[0107] Subsequently, the steps b2 - b4 are repeated so that the the multiplication coefficients to be multiplied with digital color signals R, G, B in the multipliers 32R, 32G, 32B are reduced gradually. At this moment, if it is determined at the step b2 that each of the multiplication coefficients preset in the multipliers 32R, 32G, 32B has already become equal to the brightness reducing multiplication coefficient Kref, the reducing process is stopped, so that the multiplication coefficients are each maintained at the brightness reducing multiplication coefficient Kref.

[0108] Now, a procedure for performing a brightness increasing treatment at the step S8 of Fig. 2 will be described in detail below.

[0109] In fact, the brightness increasing treatment is just a reversed treatment of the above-described brightness reducing treatment, and there are two kinds of methods for performing the brightness increasing treatment, with one being shown in Fig. 5 and the other in Fig. 6. In detail, the two methods may be mutually changed-over automatically or manually.

[0110] In a method shown in Fig. 5, the number of sustaining pulses applied from the row electrode driving pulse generating circuit 11 to the row electrodes Xi, Yi (i=1, 2. . . n) of the PDP 12 is increased so as to increased the number of times for discharge luminescence, thereby increasing the brightness of a picture displayed on the PDP 12 (as shown in Fig. 12).

[0111] Namely, once the brightness increasing treatment at step S8 in Fig. 2 is decided to be executed, the number of sustaining pulses is set (step c1 in Fig. 5) at an initial value N1.

[0112] Then, it is determined at step c2 whether the number of the sustaining pulses applied from the row electrode driving pulse generating circuit 11 to the row electrodes Xi, Yi (i=1, 2. . . n) of the PDP 12 has been set at the initial value N1.

[0113] If it is determined at the step c2 that the number of the sustaining pulses has already been set at the initial value N1, it is understood that the brightness increasing treatment is just in its process of being executed. On the other hand, if it is determined at step c2 that the number of the sustaining pulses has not been set at the initial value N1, the row electrode driving pulse generating circuit 11 is controlled (at step c3) to increase the number of sustaining pulses being applied to PDP 12 by a predetermined number, in accordance with a reading-out timing signal applied to the row electrode driving pulse generating circuit 11.

[0114] Then, it is determined at a step c4 whether a predetermined time for increasing the number of sustaining pulses has passed. If it is determined that said predetermined time has passed, the program returns to the step c2 so as to repeat the process beginning with step c2.

[0115] However, when the program is at the step c3, it is required that the number of sustaining pulses should not increased all at once. Further, an operation (to determine whether a predetermined time for reducing the number of sustaining pulses has passed) performed at step c4 is useful in obtaining an effect that the increasing of the number of the sustaining pulses will be gradual, thereby preventing a sudden brightening of a picture displayed on the PDP 12.

[0116] Subsequently, the steps c2 - c4 are repeated so that the number of sustaining pulses fed from the row electrode driving pulse generating circuit 11 is increased gradually. At this moment, if it is determined at the step c2 that the number of the sustaining pulses has been increased to the initial value N1, the increasing process is stopped, so that the number of the sustaining pulses are maintained at the initial value N1.

[0117] In a method shown in Fig. 6 which empploys a gradual stop of ABL (Automatic Brightness limiter), the multiplication coefficients to be multiplied with digital color signals R, G, B are made larger.

[0118] Namely, once the brightness increasing treatment at step S8 in Fig. 2 is decided to be executed, the multiplication coefficients to be multiplied with the digital color signals R, G, B in the multipliers 32R, 32G, 32B are each set (step d1 in Fig. 6) to be equal to an initial value K1.

[0119] Then, it is determined at a step d2 whether the multiplication coefficients set in the multipliers 32R, 32G, 32B are each equal to an initial value K1.

[0120] If it is determined at the step d2 that the multiplication coefficients set in the multipliers 32R, 32G, 32B are each equal to an initial value K1, it is understood that the brightness increasing treatment is just in its process of being executed. On the other hand, if it is determined at step d2 that the multiplication coefficients set in the multipliers 32R, 32G, 32B are not equal to the initial value K1, the multiplication coefficients to be multiplied with digital color signals R, G, B in the multipliers 32R, 32G, 32B are each increased by a predetermined value (step d3).

[0121] Then, it is determined at a step d4 whether a predetermined time for increasing the multiplication coefficients has passed. If it is determined that said predetermined time has passed, the program returns to the step d2 so as to repeat the process beginning with step d2.

[0122] However, when the program is at the step d3, it is required that the multiplication coefficients to be multiplied with digital color signals R, G, B in the multipliers 32R, 32G, 32B should not be increased to be equal to the initial value K1 all at once. Further, an operation (to determine whether a predetermined time for increasing the multiplication coefficients has passed)

performed at at step b4 is useful in obtaining an effect of preventing a sudden brightening of a picture displayed on the PDP 12 by avoiding a sudden increasing of the brightness.

[0123] Subsequently, the steps d2 - d4 are repeated so that the the multiplication coefficients to be multiplied with digital color signals R, G, B in the Multipliers 32R, 32G, 32B are increased gradually. At this moment, if it is determined at the step d2 that each of the multiplication coefficients has already become equal to the initial value K1, the increasing process is stopped, so that the multiplication coefficients are each maintained at the initial value K1.

[0124] While the presently preferred embodiments of the this invention have been shown and described above, it is to be understood that these disclosures are for the purpose of illustration and that various changes and modifications may be made without departing from the scope of the invention as set forth in the appended claims.

Claims

1. A method of controlling a brightness of a picture displayed on a plasma display panel by increasing or decreasing said brightness, said method comprising:

   determining whether a video signal to be fed to the plasma display panel is a signal indicating a stationary picture;
   reducing the brightness of a picture displayed on the plasma display panel if it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture.

2. The method according to claim 1, wherein one average brightness level of a video signal to be fed to the plasma display panel is detected during a predetermined period, said one average brightness level is then compared with a former average brightness level detected immediately before the detection of said one average brightness level, so as to obtain a difference between said one average brightness level and said former average brightness level.

3. The method according to claim 2, wherein when the difference between said one average brightness level and said former average brightness level is smaller than a predetermined value and such condition has continued for a predetermined time, it is determined that said video signal is a signal indicating a stationary picture.

4. The method according to claim 1, wherein when it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture, the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel is reduced.

5. The method according to claim 4, wherein the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel is reduced gradually step by step.

6. The method according to claim 1, wherein when it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture, multiplication coefficients are made smaller which will be multiplied with video signals to be fed to the plasma display panel to adjust the brightness of the stationary picture displayed on the plasma display panel.

7. A system for controlling a brightness of a picture displayed on a plasma display panel by increasing or decreasing said brightness, said system comprising:

   determining means for determining whether a video signal to be fed to the plasma display panel is a signal indicating a stationary picture;
   brightness reducing means for reducing the brightness of a picture displayed on the plasma display panel if it is determined that a video signal to be fed to the plasma display panel is a signal indicating a stationary picture.

8. The system according to claim 7, wherein the determining means comprises:

   average brightness level detecting means for detecting during a predetermined period one average brightness level of a video signal to be fed to the plasma display panel;
   calculating means for comparing said one average brightness level with a former average brightness level detected immediately before the detection of said one average brightness level and for obtaining a difference between said one average brightness level and said former average brightness level;
   monitor means for monitorring whether the difference obtained by the calculating means has continuously been smaller than a predetermined value for a predetermined time;
   wherein when the monitor means determines that the difference obtained by the calculating means has continuously been smaller than a predetermined value for a predetermined time, it is determined that said video signal is a signal indicating a stationary picture.

9. The method according to claim 7, wherein the brightness reducing means is means capable of reducing the number of sustaining pulses for maintaining luminescent discharge on the plasma display panel.

10. The method according to claim 9, wherein the brightness reducing means is capable of reducing the number of the sustaining pulses gradually step by step.

11. The method according to claim 7, wherein the brightness reducing means is means capable of reducing multiplication coefficients to be multiplied by video signals to be fed to the plasma display panel so as to adjust the brightness level of the video signals.

FIG.1

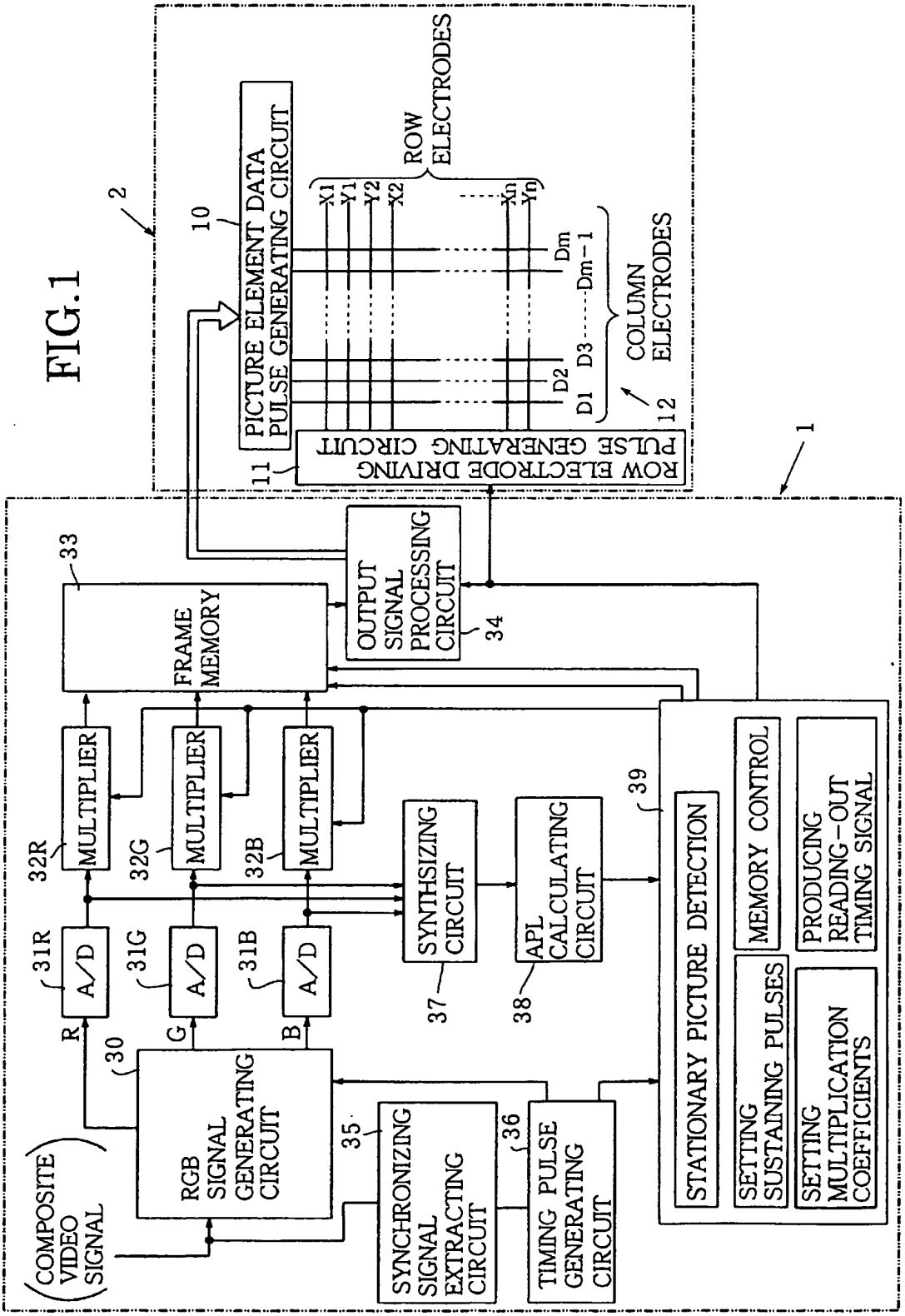

2
10
PICTURE ELEMENT DATA PULSE GENERATING CIRCUIT
ROW ELECTRODES
X1
Y1
Y2
X2
Xn
Yn
Dm
Dm-1
D3
D2
D1
COLUMN ELECTRODES
12
11
ROW ELECTRODE DRIVING PULSE GENERATING CIRCUIT
1
33
FRAME MEMORY
OUTPUT SIGNAL PROCESSING CIRCUIT
34
32R
32G
32B
MULTIPLIER
MULTIPLIER
MULTIPLIER
31R
31G
31B
A/D
A/D
A/D
R
G
B
30
RGB SIGNAL GENERATING CIRCUIT
COMPOSITE VIDEO SIGNAL
35
SYNCHRONIZING SIGNAL EXTRACTING CIRCUIT
36
TIMING PULSE GENERATING CIRCUIT
37
SYNTHSIZING CIRCUIT
38
APL CALCULATING CIRCUIT
39
STATIONARY PICTURE DETECTION
SETTING SUSTAINING PULSES
SETTING MULTIPLICATION COEFFICIENTS
MEMORY CONTROL
PRODUCING READING-OUT TIMING SIGNAL

FIG.2

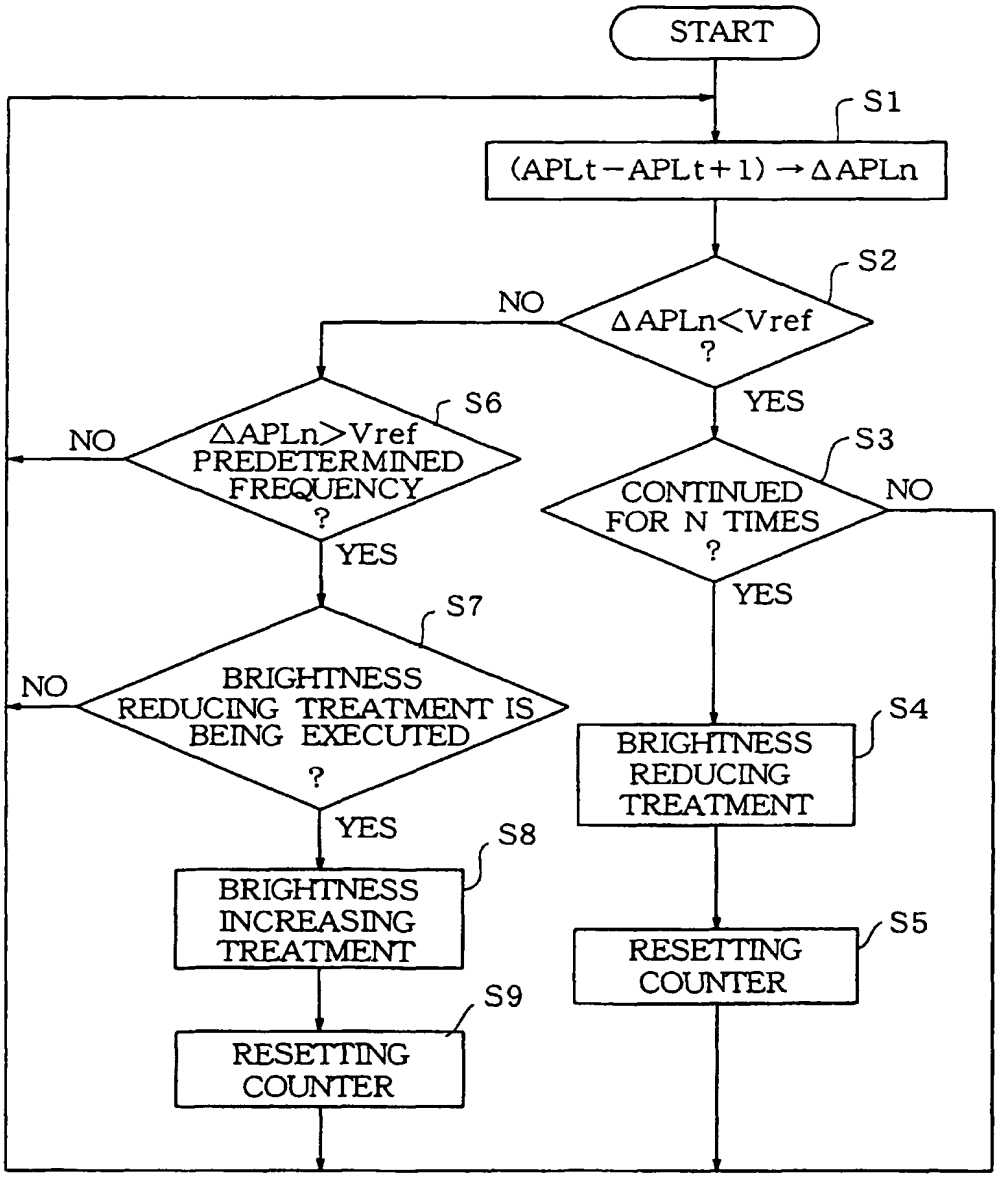

START
S1
(APLt−APLt+1)→ΔAPLn
S2
NO
ΔAPLn<Vref ?
YES
S6
NO
ΔAPLn>Vref PREDETERMINED FREQUENCY ?
S3
CONTINUED FOR N TIMES ?
NO
YES
YES
S7
NO
BRIGHTNESS REDUCING TREATMENT IS BEING EXECUTED ?
S4
BRIGHTNESS REDUCING TREATMENT
YES
S8
BRIGHTNESS INCREASING TREATMENT
S5
RESETTING COUNTER
S9
RESETTING COUNTER

FIG.3

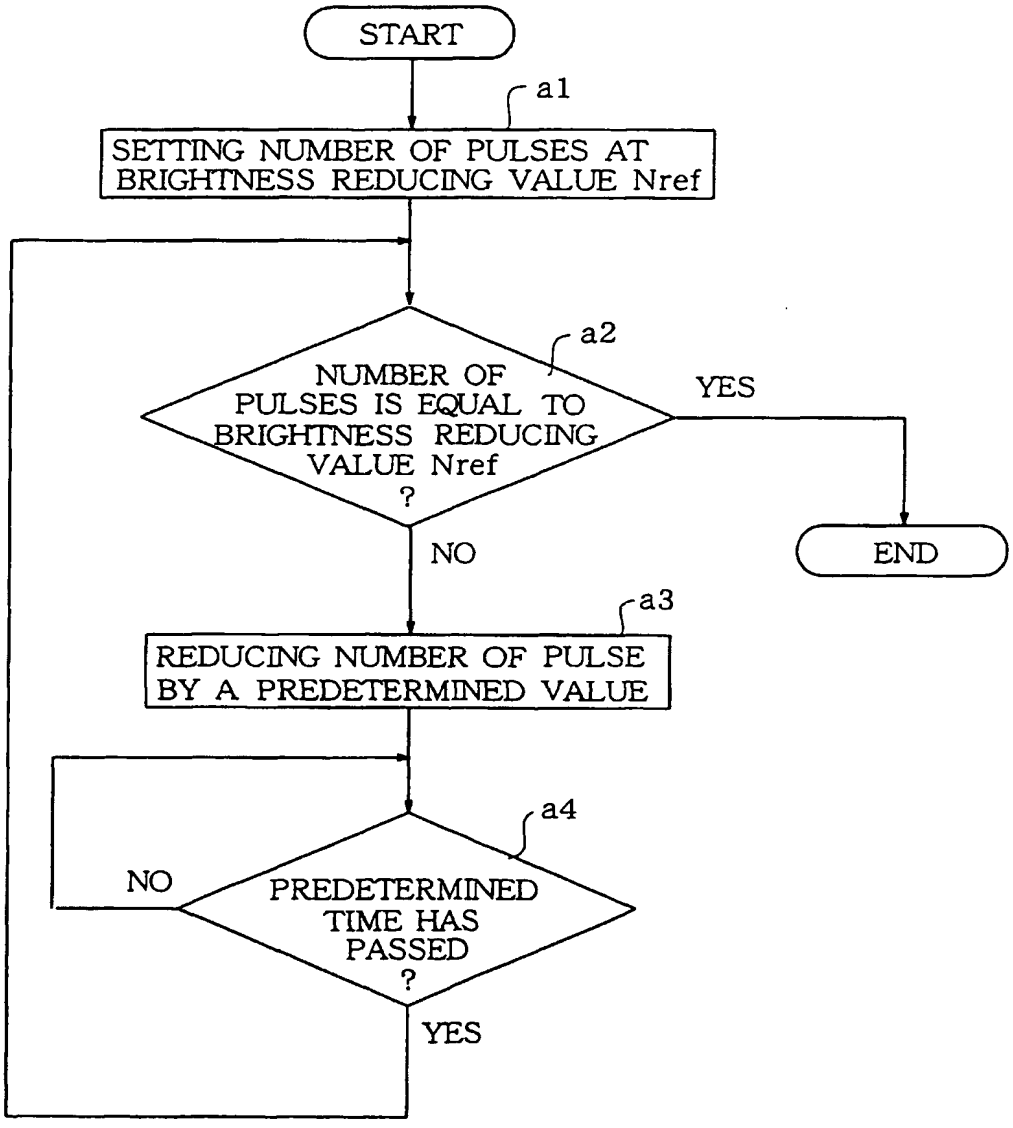

START
a1
SETTING NUMBER OF PULSES AT BRIGHTNESS REDUCING VALUE Nref
a2
NUMBER OF PULSES IS EQUAL TO BRIGHTNESS REDUCING VALUE Nref ?
YES
NO
END
a3
REDUCING NUMBER OF PULSE BY A PREDETERMINED VALUE
a4
NO
PREDETERMINED TIME HAS PASSED ?
YES

FIG.4

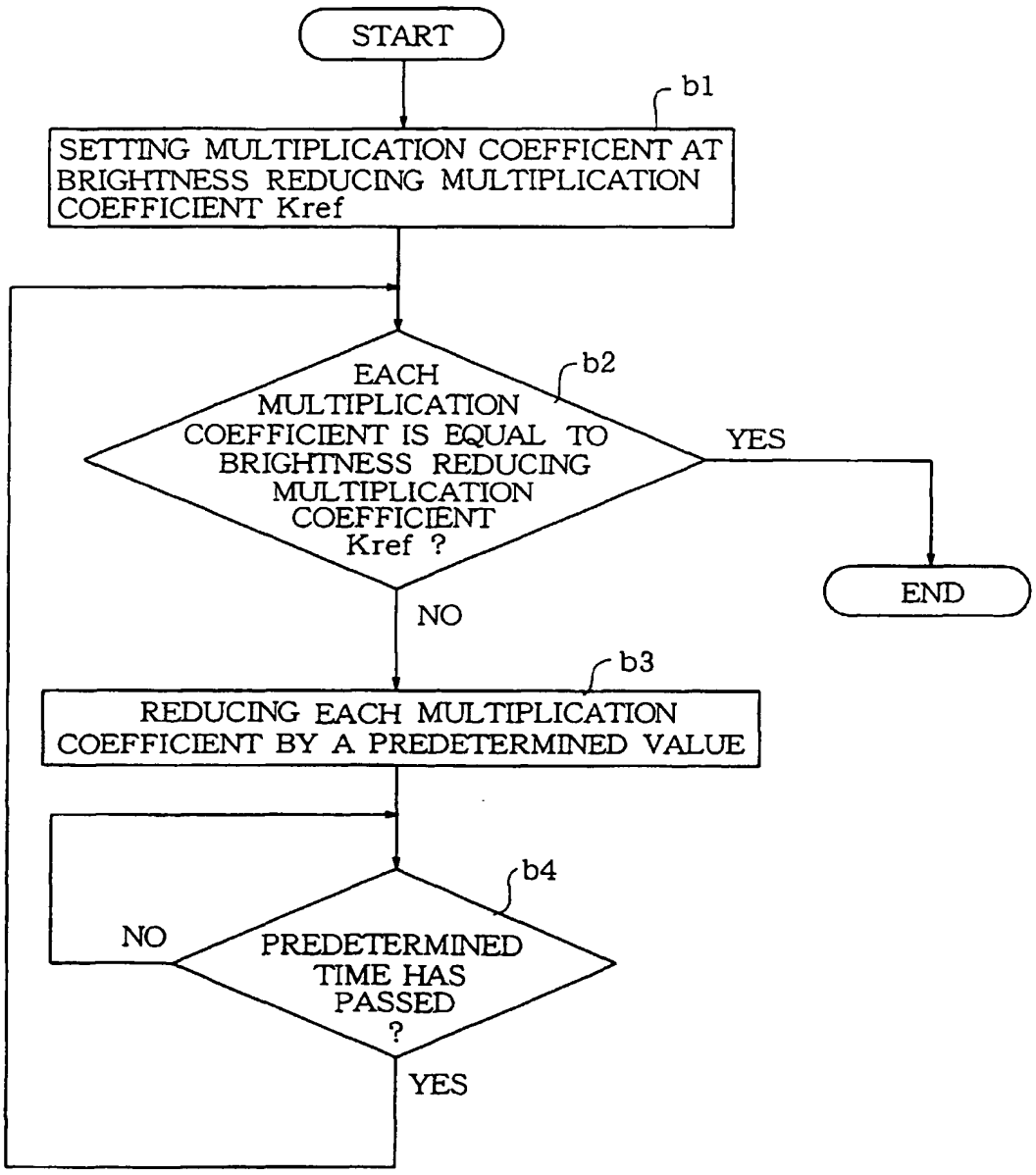

START
b1
SETTING MULTIPLICATION COEFFICENT AT BRIGHTNESS REDUCING MULTIPLICATION COEFFICIENT Kref
b2
EACH MULTIPLICATION COEFFICIENT IS EQUAL TO BRIGHTNESS REDUCING MULTIPLICATION COEFFICIENT Kref ?
YES
END
NO
b3
REDUCING EACH MULTIPLICATION COEFFICIENT BY A PREDETERMINED VALUE
b4
NO
PREDETERMINED TIME HAS PASSED ?
YES

FIG.5

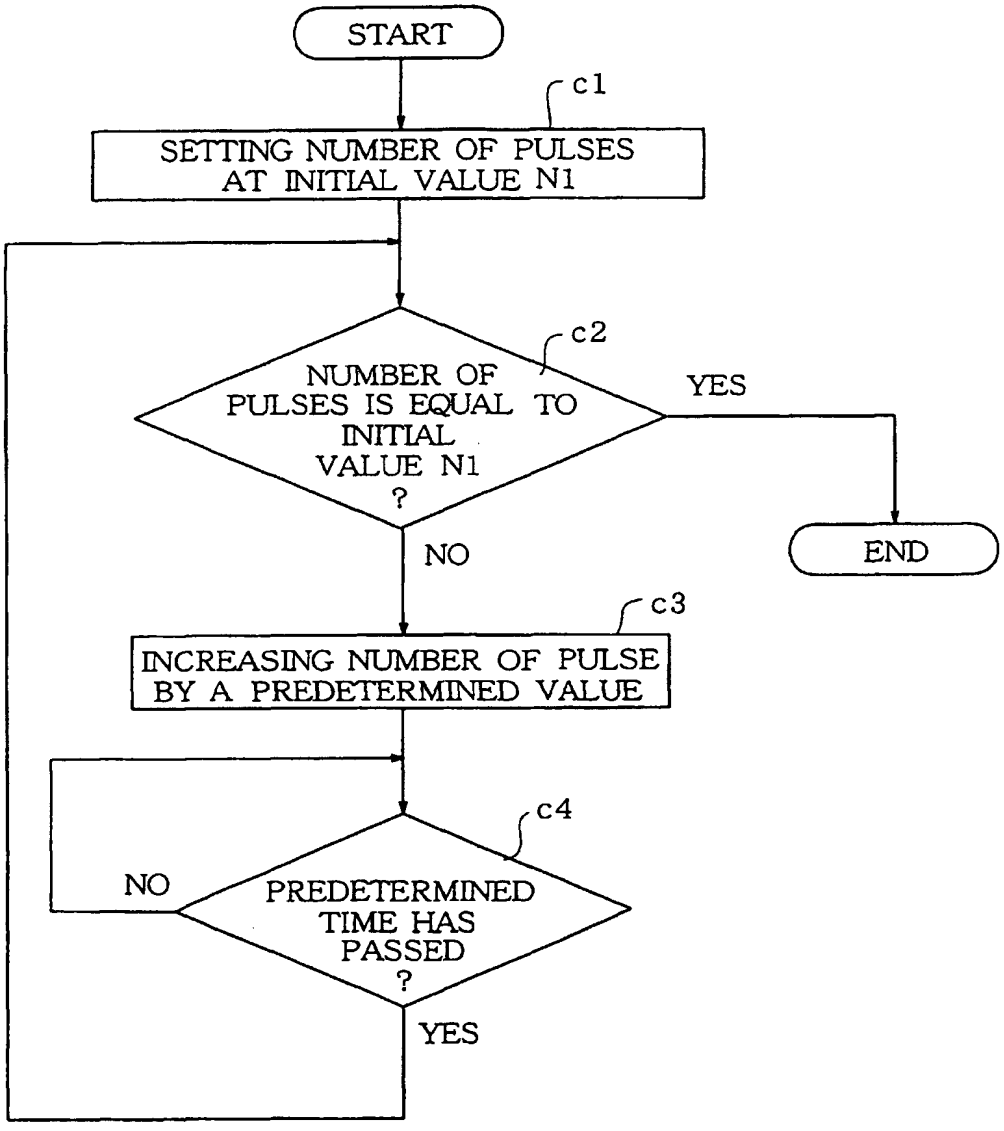

START
c1
SETTING NUMBER OF PULSES AT INITIAL VALUE N1
c2
NUMBER OF PULSES IS EQUAL TO INITIAL VALUE N1 ?
YES
END
NO
c3
INCREASING NUMBER OF PULSE BY A PREDETERMINED VALUE
c4
NO
PREDETERMINED TIME HAS PASSED ?
YES

FIG.6

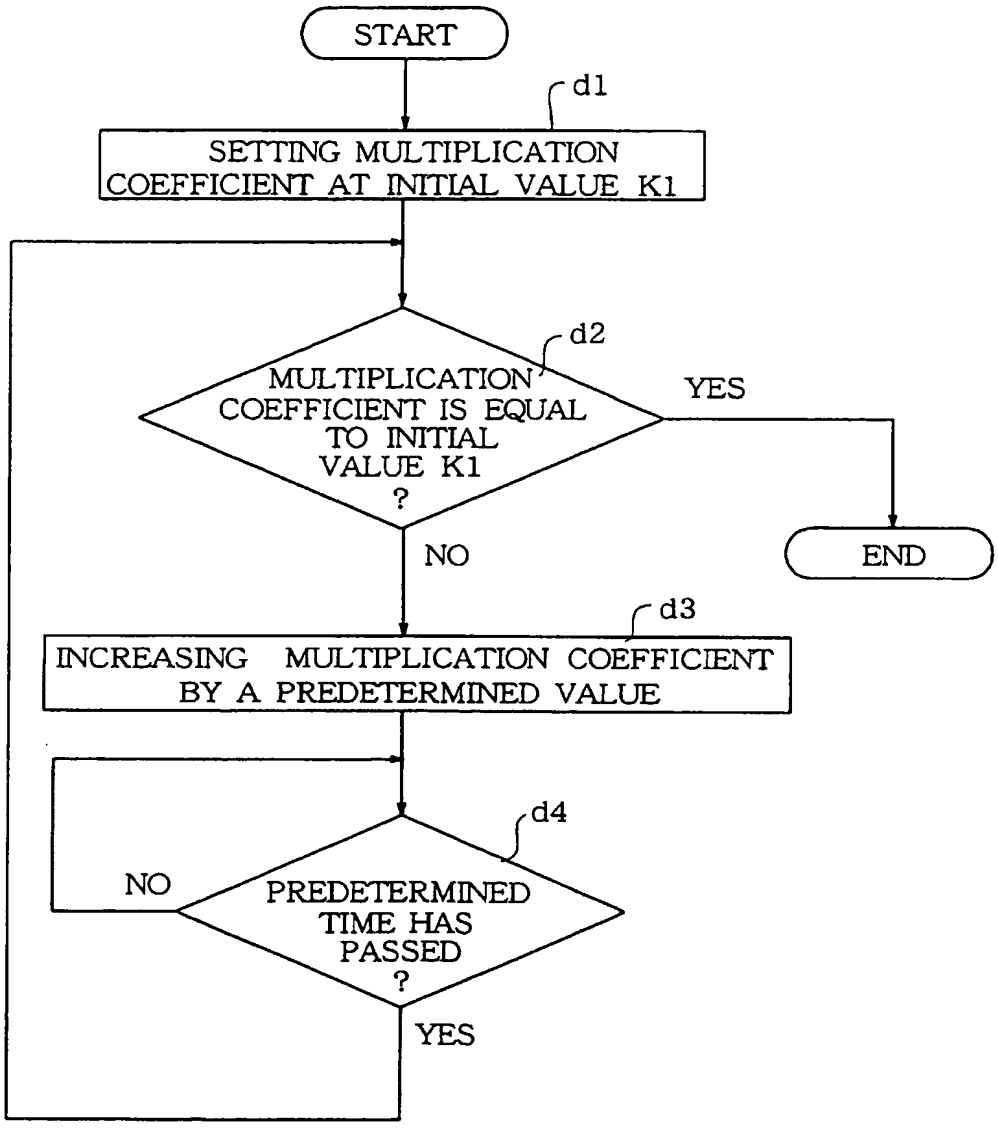

START
d1
SETTING MULTIPLICATION COEFFICIENT AT INITIAL VALUE K1
d2
MULTIPLICATION COEFFICIENT IS EQUAL TO INITIAL VALUE K1 ?
YES
NO
END
d3
INCREASING MULTIPLICATION COEFFICIENT BY A PREDETERMINED VALUE
d4
NO
PREDETERMINED TIME HAS PASSED ?
YES

FIG.7

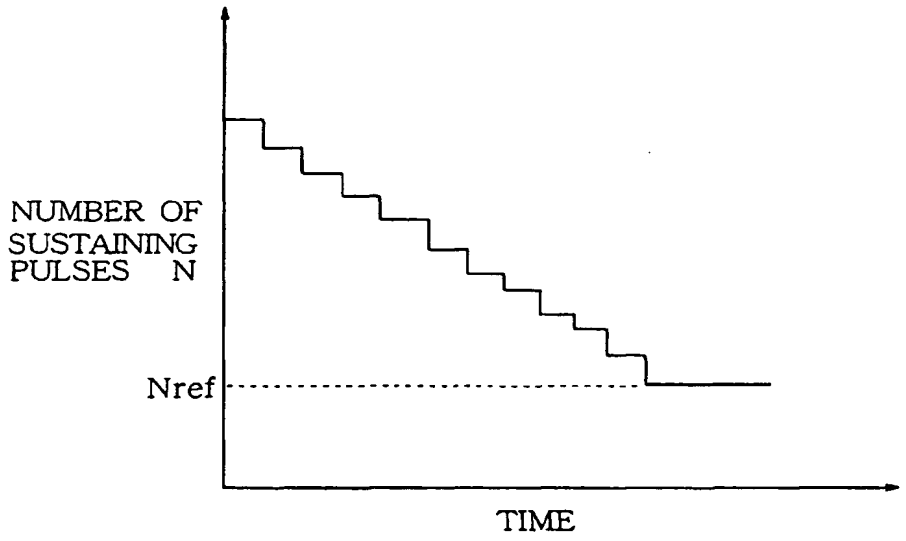


FIG.8

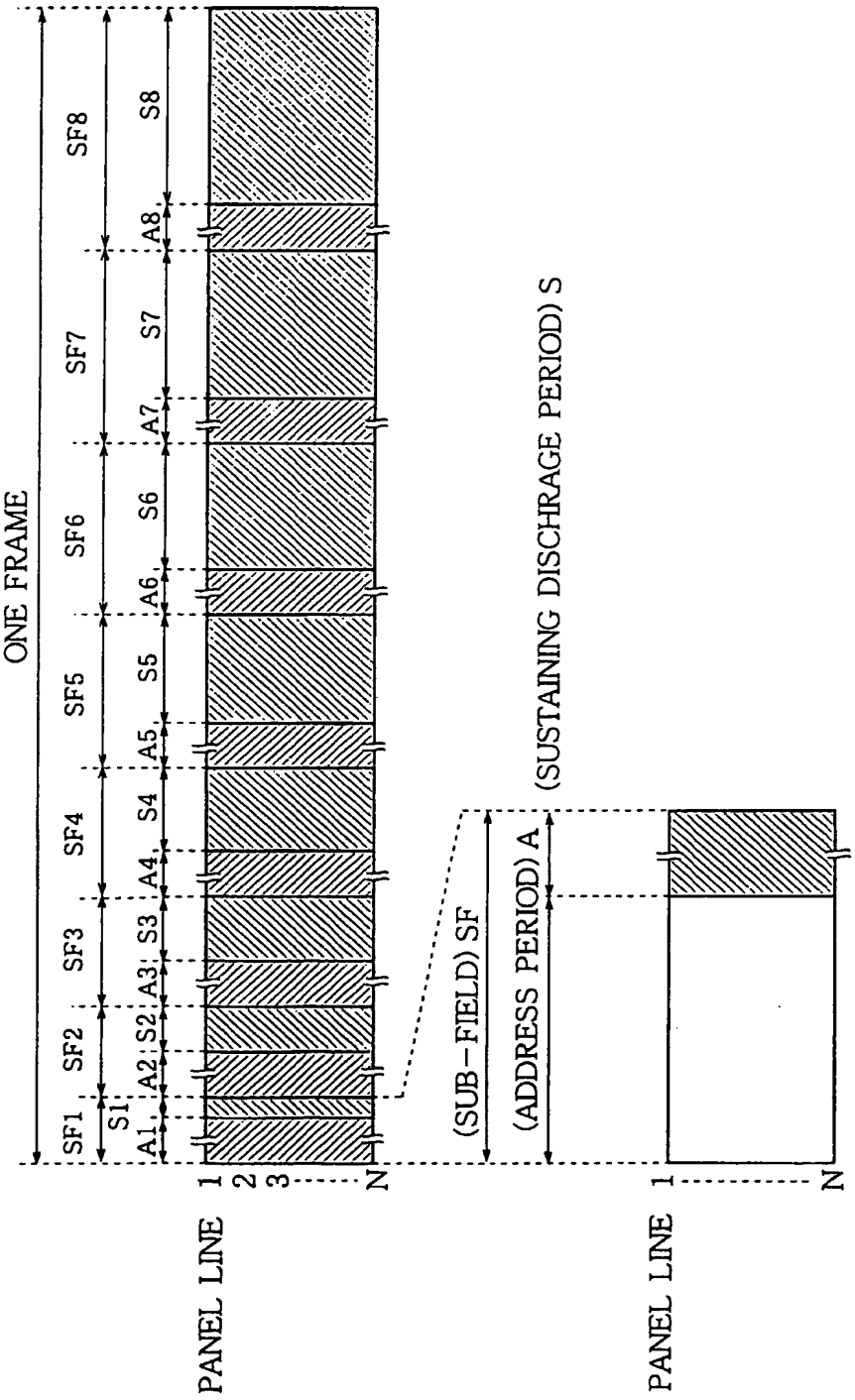

ONE FRAME
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
S1
S2
S3
S4
S5
S6
S7
S8
A1
A2
A3
A4
A5
A6
A7
A8
PANEL LINE
1
2
3
N
(SUB-FIELD) SF
(ADDRESS PERIOD) A
(SUSTAINING DISCHRAGE PERIOD) S
PANEL LINE
1
N

FIG.9

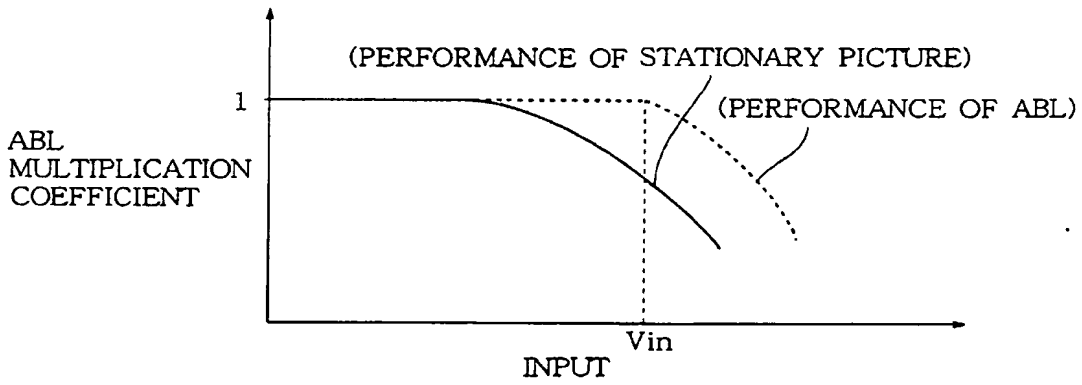

(PERFORMANCE OF STATIONARY PICTURE)
(PERFORMANCE OF ABL)
1
ABL
MULTIPLICATION
COEFFICIENT
Vin
INPUT

FIG.10

PRIOR ART

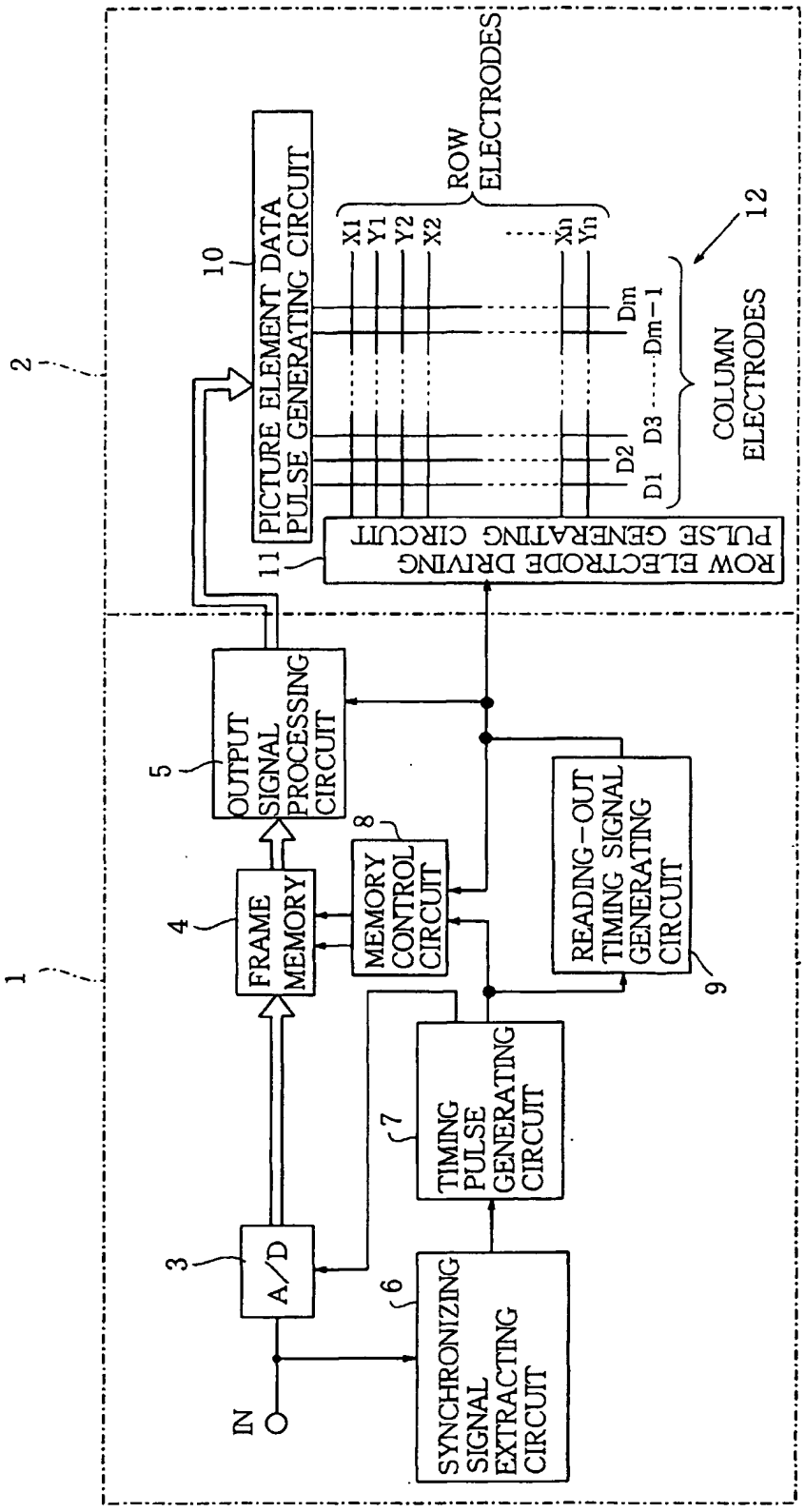


FIG.11

PRIOR ART

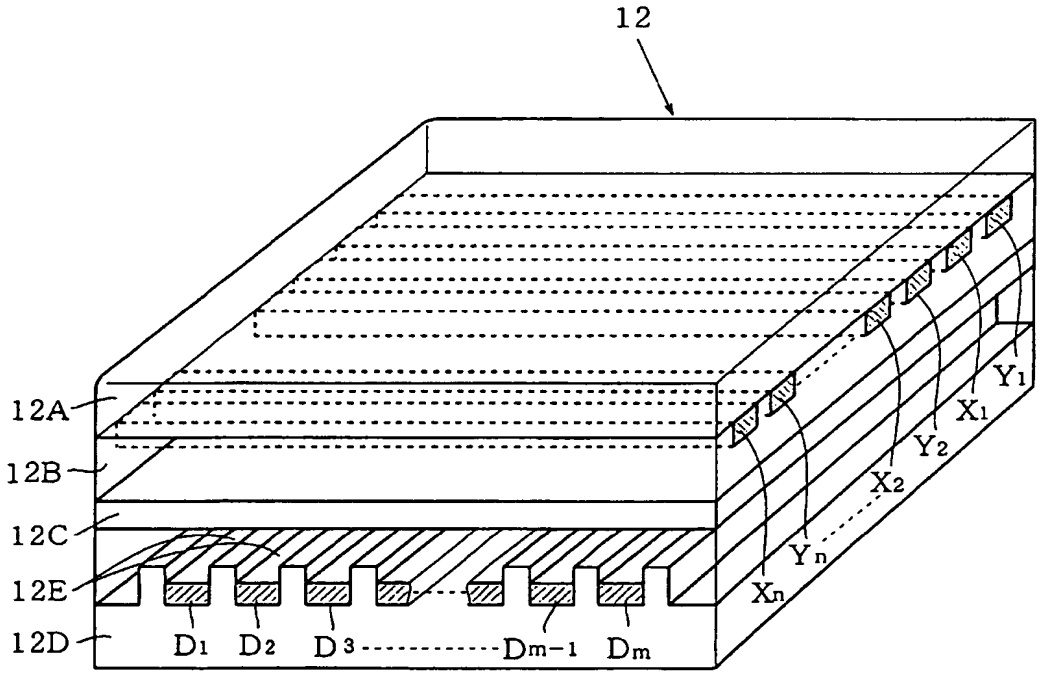


FIG.12

PRIOR ART

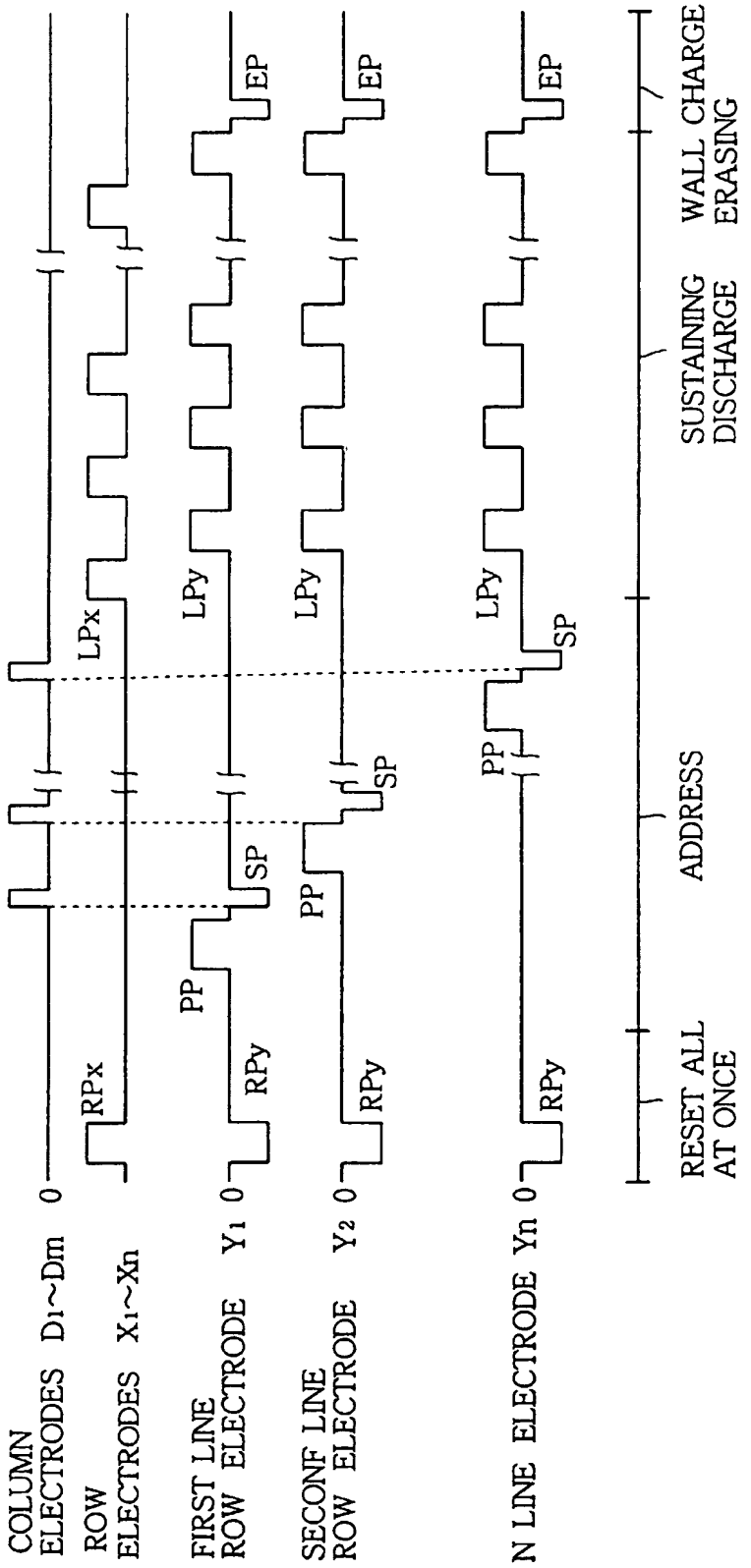


FIG.13

PRIOR ART

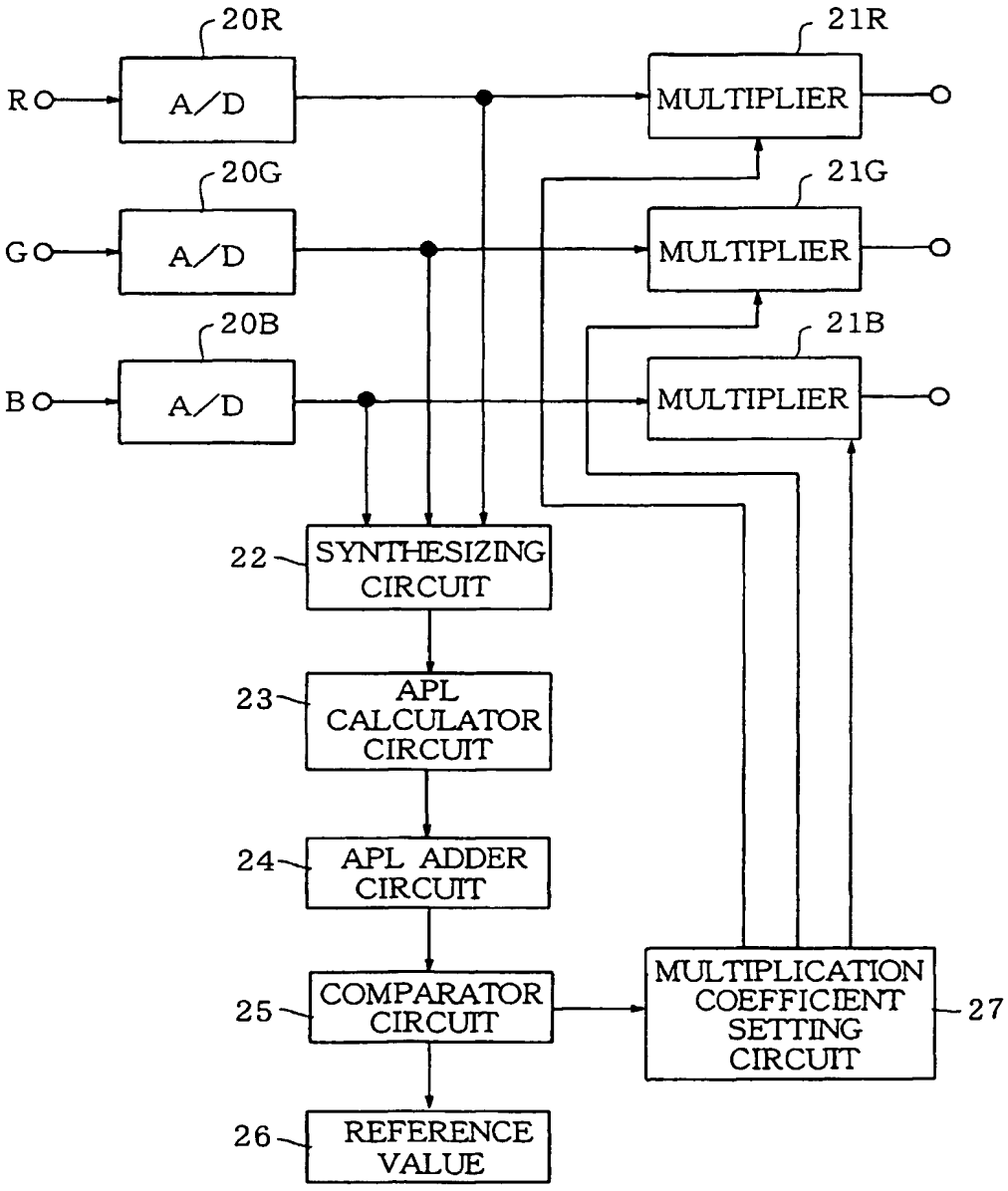


FIG.14 A

PRIOR ART

1	128/255
2	200/255
3	128/255
4	200/255
5	128/255
6	200/255
7	128/255
8	200/255

FIG.14 B

PRIOR ART

1	128/255
2	128/255
3	128/255
4	200/255
5	200/255
6	128/255
7	128/255
8	128/255

FIG.14 C

PRIOR ART

1	64/255
2	64/255
3	64/255
4	100/255
5	100/255
6	64/255
7	64/255
8	64/255

FIG.15

PRIOR ART

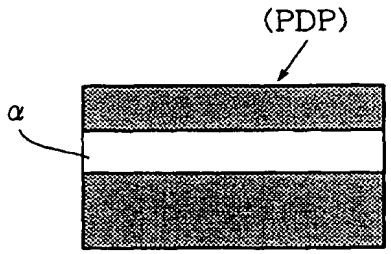
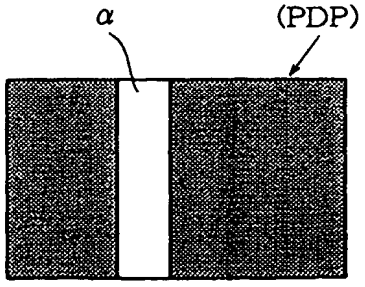


FIG.16

PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 11 1657

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	EP 0 841 652 A (FUJITSU LTD.) 13 May 1998 (1998-05-13) * abstract * * column 1, line 51 - column 2, line 13 * * column 13, line 37 - line 52; figure 23 * ---	1,4,5,7, 9,10 2,3,6,11	G09G3/28
A	PATENT ABSTRACTS OF JAPAN vol. 96, no. 7, 31 July 1996 (1996-07-31) & JP 008 065607 A (FUJITSU GENERAL LTD.), 8 March 1996 (1996-03-08) * abstract * ---	1-11	
A	US 5 757 343 A (NAGAKUBO) 26 May 1998 (1998-05-26) * column 8, line 55 - column 9, line 33; figure 10 * -----	1-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 October 1999	O'Reilly, D

CATEGORY OF CITED DOCUMENTS

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01-10-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 841652 A	13-05-1998	JP 2900997 B	02-06-1999
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JP 008065607 A	08-03-1996	NONE	
US 5757343 A	26-05-1998	JP 8286636 A	01-11-1996

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